REMARKS

This is intended as a full and complete response to the Final Office Action dated June 16, 2005, having a shortened statutory period for response set to expire on September 16, 2005. Applicants submit this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-26 are pending in the application. Claims 1, 12, 19, and 23 have been amended to clarify the subject matter claimed. Applicants respectfully submit that the claim amendments do not introduce new matter. Claims 1-26 remain pending following entry of this response.

Claim Rejections - 35 U.S.C. § 102

Claims 1-26 are rejected under 35 U.S.C. 102(b) as being anticipated by *McMahan et al.* (U.S. 5,337,269, hereinafter "*McMahan*"). Applicants respectfully traverse this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Applicants maintain that *McMahan* does not disclose "each and every element as set forth in the claim".

With respect to claims 1 and 12, the claims recite at least first and second sub-ALUs, each sub-ALU configured to operate on at least two multi-bit numbers to generate a multi-bit numerical result, wherein the slices of the first and second sub-ALUs are interleaved. *See, e.g.* Claim 1. Examiner argues that *McMahan* discloses first ALUs in Figure 1, gates 14a-14e and alternatively in Figure 2, blocks 22a-22e. In fact, the cited gates 14a-14e and blocks 22a-22e are portions of a carry skip adder, and are used to propagate a single bit skip carry term, SC within the adder, and do not

generate a multi-bit numerical result, as claimed. *See* Figure 1, Figure 2, Col. 3, Lines 61-77; Col. 4, Lines 4-44.

Therefore, Applicant submits *McMahan* does not anticipate claims 1 and 12. Accordingly, Applicant submits claims 1, 12, and their dependents are allowable and respectfully request withdrawal of this rejection with respect to these claims.

With respect to claims 19 and 23, the claims recite at least first and second ALUs, each ALU configured to operate on at least two multi-bit numbers to generate a multi-bit numerical result. Examiner argues that gates 14a-14g depicted in Figure 1 of *McMahan* are a second ALU. As above, Applicant's maintain that the elements cited by are used to propagate a single bit skip carry signal. *See* Col. 4, Lines 4-27. Accordingly, *McMahan* does not disclose at least first and second ALUs, each ALU configured to operate on at least two multi-bit numbers to generate a multi-bit numerical result. Therefore, the rejection is believed to be overcome.

Furthermore, with respect to Examiner's rejection of claims 19 and 23, Applicants submit that an adder is part of an ALU. *See* "Adder" *defined at* www.wikipedia.org. Thus, the components of a single carry skip adder, cited by Examiner, are not separate ALUs, but may merely form part of a single ALU. *Id. McMahan* itself recognizes that an adder is part of an ALU and does not form multiple ALUs, stating "design-adders are central to ALU design." *See* Col. 1, Lines 15-16. Accordingly, *McMahan* does not disclose at least first and second ALUs, each ALU configured to operate on at least two multi-bit numbers to generate a multi-bit numerical result.

Also, with respect to claims 19 and 23, the claims describe arranging the first and second ALUs using one of first and second arrangements, wherein the first arrangement comprises arranging the first output side closer to the second output side than to the second input side, the second arrangement comprises arranging the first input side closer to the second input side than to the second output side. Thus, the pending claims are directed to a physical arrangement of first and second ALUs. The figures cited by Examiner and the text describing the figures do not disclose any physical arrangement of the depicted components. *See* Figure 1, Figure 2, Col. 3 Line 61 – Col. 4, Line 68. Figures 1 and 2 of *McMahan* are in fact directed to the logical connections of the components, and not to a physical relationship among the

components. *See id.* Accordingly, *McMahan* does not disclose arranging the first and second ALUs using one of first and second arrangements, wherein the first arrangement comprises arranging the first output side closer to the second output side than to the second input side, the second arrangement comprises arranging the first input side closer to the second input side than to the second output side.

Therefore, Applicant submits *McMahan* does not anticipate claims 19 and 23. Accordingly, Applicant submits claims 19, 23, and their dependents are allowable and respectfully request withdrawal of this rejection with respect to these claims.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact the undersigned attorney to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted,

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